basic education

Department:
Basic Education
**REPUBLIC OF SOUTH AFRICA**

# SENIOR CERTIFICATE EXAMINATIONS/ NATIONAL SENIOR CERTIFICATE EXAMINATIONS

## ELECTRICAL TECHNOLOGY: DIGITAL ELECTRONICS

## 2023

**MARKS: 200**

**TIME: 3 hours**

**This question paper consists of 16 pages, a 1-page formula sheet and an 8-page answer sheet.**

## INSTRUCTIONS AND INFORMATION

1. This question paper consists of SIX questions.

2. Answer ALL the questions.

3. Answer the following questions on the attached ANSWER SHEETS:

   QUESTIONS 3.3.6, 3.4.3 and 3.6.1
   QUESTIONS 5.2.1, 5.2.2, 5.4.1, 5.4.3, 5.6.2 and 5.7
   QUESTION 6.9

4. Write your centre number and examination number on every ANSWER SHEET and hand them in with your ANSWER BOOK, whether you have used them or not.

5. Sketches and diagrams must be large, neat and FULLY LABELLED.

6. Show ALL calculations and round off answers correctly to TWO decimal places.

7. Number the answers correctly according to the numbering system used in this question paper.

8. You may use a non-programmable calculator.

9. Calculations must include:

   9.1 Formulae and manipulations where needed

   9.2 Correct replacement of values

   9.3 Correct answer and relevant units where applicable

10. A formula sheet is attached at the end of this question paper.

11. Write neatly and legibly.

## QUESTION 1: MULTIPLE-CHOICE QUESTIONS

Various options are provided as possible answers to the following questions. Choose the answer and write only the letter (A–D) next to the question numbers (1.1 to 1.15) in the ANSWER BOOK, e.g. 1.16 D.

1.1 A critical incident causes …

A damage to equipment. External repair services are required.
B a person to sustain a sudden and severe physical injury. External medical services are required.
C a person to sustain a physical injury. External medical services are not required.
D a person to get a mental disturbance. A restful recovery is required. (1)

1.2 The operation of a Schmitt trigger can best be described by …

A hysteresis.
B negative feedback.
C open-loop gain.
D attenuation. (1)

1.3 The … is the only op-amp application that uses an 'open loop' connection to bring its full gain of ±100 000 into use.

A summing amplifier
B integrator
C comparator
D differentiator (1)

1.4 The … determines the shape of the output in an op-amp integrator circuit.

A input capacitor
B feedback resistor
C input voltage
D RC time constant (1)

1.5 When a square wave is fed to the input of a passive RC differentiator with a short time constant, the output will be a …

A sine wave with 90º phase shift.
B spike with a fast rise and slow decay.
C square wave with 180º phase shift.
D a triangular wave. (1)

1.6 ONE of the characteristics of an ideal op amp is that the input impedance is …

A extremely high.
B zero.
C extremely low.
D moderate. (1)

1.7 When negative feedback is used in an op-amp circuit, the overall gain is …

A increased.
B unchanged.
C reduced.
D infinite. (1)

1.8 When the anodes of all eight LEDs are connected together to a single positive voltage rail, it is called a common ….

A cathode.
B anode.
C display.
D neutral. (1)

1.9 A combinational logic circuit which combines an AND gate with an exclusive OR gate is called a …

A full adder.
B parallel adder.
C half adder.
D binary adder. (1)

1.10 A clocked RS flip-flop is in a reset condition when …

A S = 1, R = 1
B S = 1, R = 0
C S = 0, R = 1
D S = 0, R = 0 (1)

1.11 The process where the timing signal is delayed by a fraction through each flip-flop is known as …

A transmission delay.
B propagation delay.
C queuing delay.
D processing delay. (1)

1.12 A register where all four bits of data are introduced to the register at the same time but, once stored, they are shifted out of the register one bit at a time is called …

A parallel-in: parallel-out.
B series-in: series-out.
C parallel-in: series-out.
D series-in: parallel-out. (1)

1.13 The term ROM means … with reference to microcontrollers.

A read-only memory
B read-output memory
C read-onset memory
D random only memory (1)

1.14 The term 'SPI' stands for …

A serial peripheral interface.
B standard parallel interface.
C serial pathway interface.
D standard processor interface. (1)

1.15 The process that allows a task to be repeated multiple times is called ….

A debugging.
B data flow lines.
C looping.
D a flow diagram. (1)
**[15]**

## QUESTION 2: OCCUPATIONAL HEALTH AND SAFETY

2.1 State the purpose of the Occupational Health and Safety Act, 1993 (Act 85 of 1993). (3)

2.2 Explain how an *unsafe act* can reduce the rate of production at the work place. (2)

2.3 Explain the term *high impact; low probability* with reference to risk analysis. (2)

2.4 State TWO recommended procedures to stop bleeding in an emergency. (2)

2.5 State ONE procedure to follow for personal protection when administering the procedures mentioned in QUESTION 2.4. (1)
**[10]**

## QUESTION 3: SWITCHING CIRCUITS

3.1 FIGURE 3.1 below shows block diagrams with different input and output states for three types of multivibrators. Identify the multivibrator in each of the following blocks:

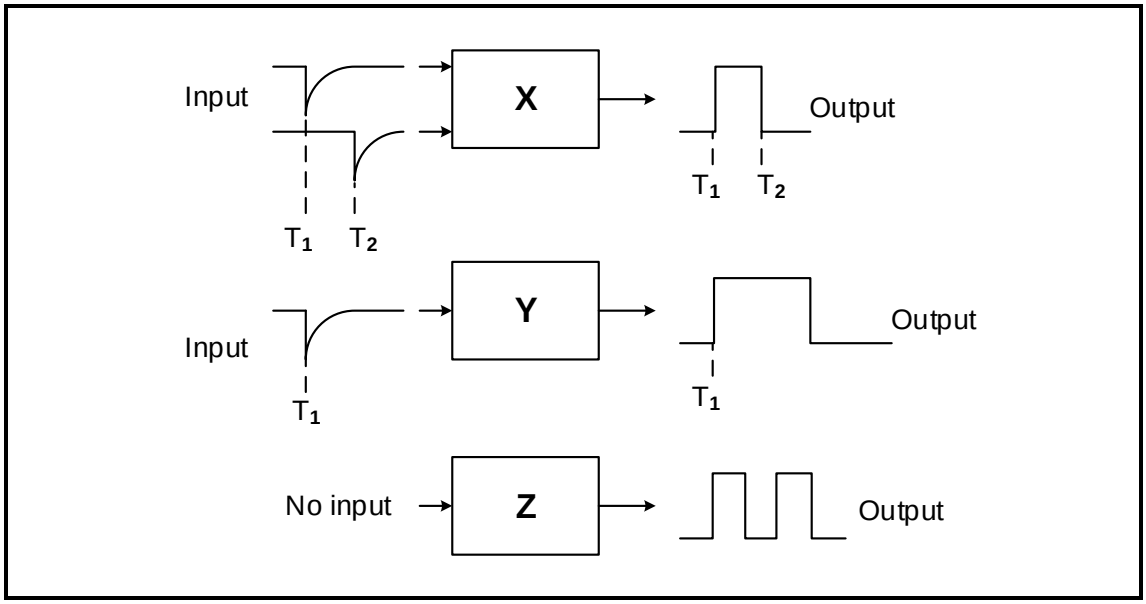



**FIGURE 3.1: BLOCK DIAGRAMS OF MULTIVIBRATORS**

3.1.1 Block **X** (1)

3.1.2 Block **Y** (1)

3.1.3 Block **Z** (1)

3.2 FIGURE 3.2 below shows the circuit of a multivibrator. Answer the questions that follow.

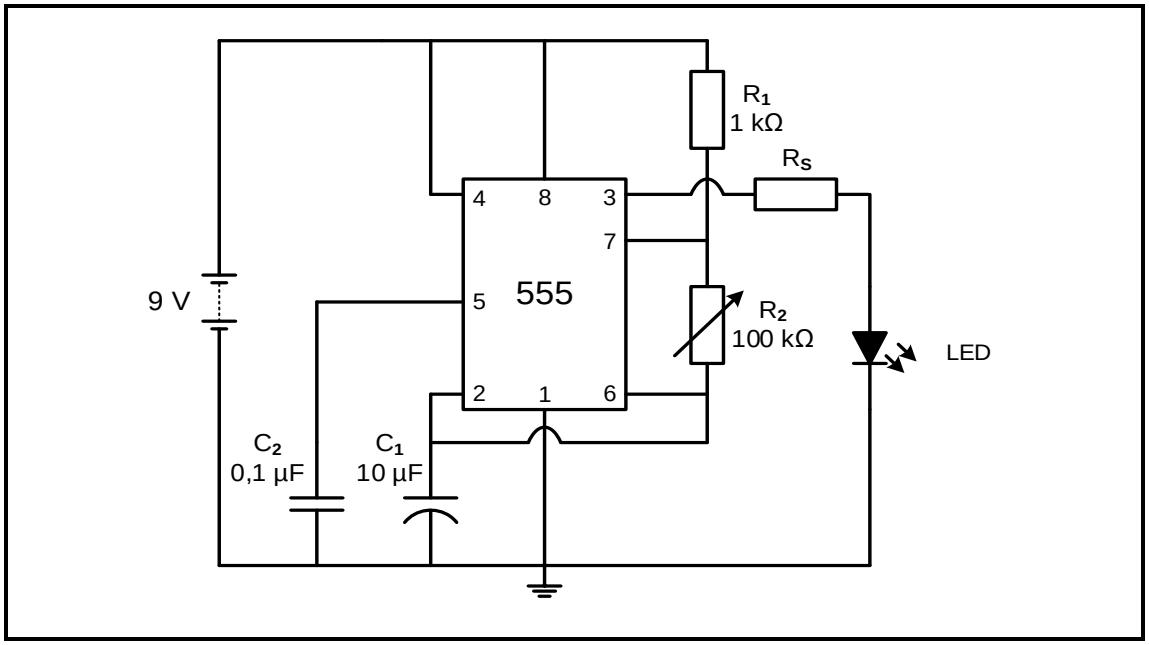



**FIGURE 3.2: MULTIVIBRATOR CIRCUIT**

3.2.1 State the purpose of the variable resistor $R_2$. (2)

3.2.2 Explain how the LED will be affected if it is directly connected to pin 3 without resistor $R_S$. (3)

3.2.3 Explain how this circuit operates. (4)

3.2.4 State the discharge path of capacitor $C_1$. (1)

3.3 FIGURE 3.3 below shows a monostable multivibrator circuit using a 741 op amp. The capacitor is fully charged through resistor $R_3$. Answer the questions that follow.

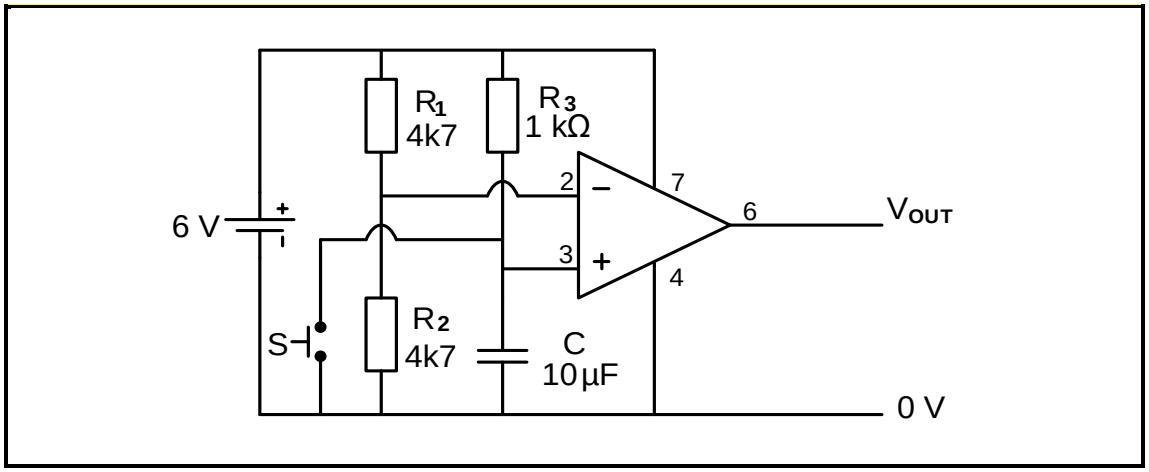



**FIGURE 3.3: MONOSTABLE MULTIVIBRATOR CIRCUIT**

3.3.1 Determine the voltage at pin 2 (inverting input) of the op amp. (2)

3.3.2 Determine the voltage at pin 3 (non-inverting input) when the switch is open. (1)

3.3.3 State whether the output is high (6 V) or low (0 V) when the switch is open. Motivate your answer. (2)

3.3.4 Determine the voltage at pin 3 (non-inverting input) when the switch is pressed. Motivate your answer. (2)

3.3.5 Describe the operation of the circuit with reference to the voltages on the two input terminals and the output of the op amp when the switch is pressed. (5)

3.3.6 Refer to FIGURE 3.3.6 below and draw the output waveform on the ANSWER SHEET for QUESTION 3.3.6.

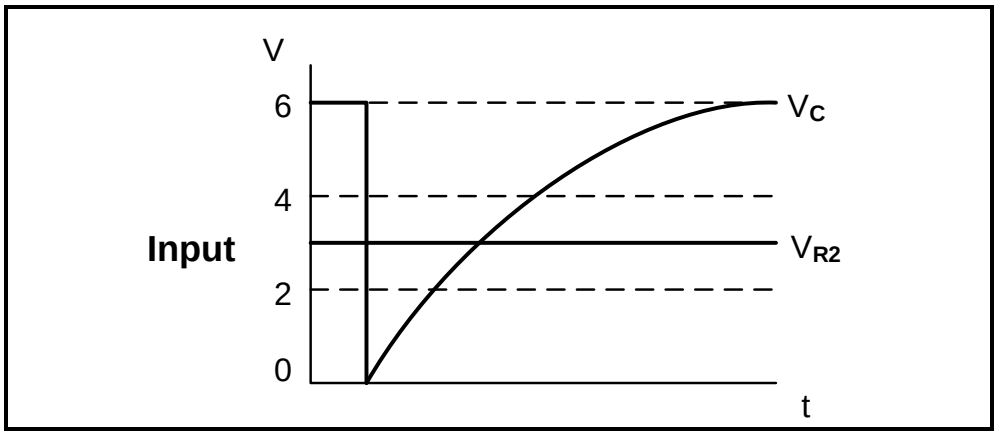



**FIGURE 3.3.6** (3)

3.4 FIGURE 3.4 below shows a non-inverting Schmitt trigger. Answer the questions that follow.

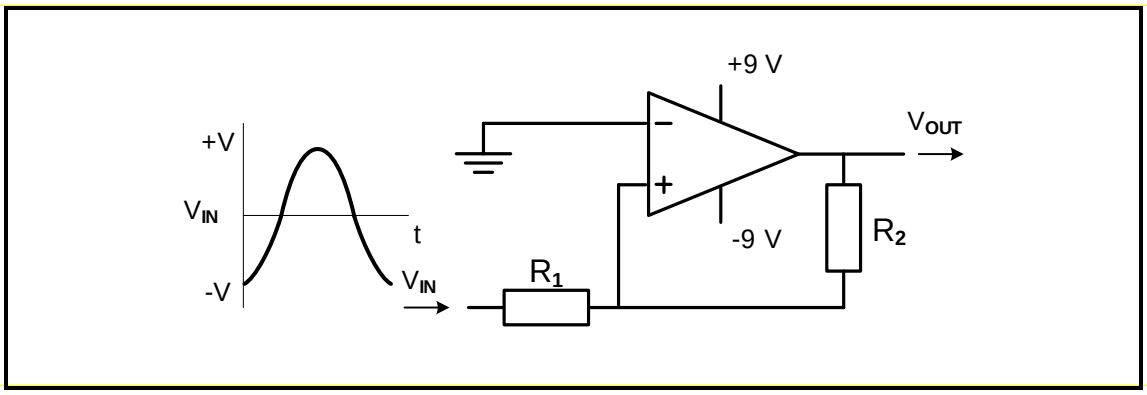



**FIGURE 3.4: NON-INVERTING SCHMITT TRIGGER**

3.4.1 Determine the voltage at which the circuit will trigger. Motivate your answer. (2)

3.4.2 Name TWO uses of a Schmitt trigger. (2)

3.4.3 Draw the output signal on the ANSWER SHEET for QUESTION 3.4.3. (4)

3.5 The information in TABLE 3.5 below was gathered from an inverting summing amplifier with three inputs. The input resistors are all equal and the feedback resistance was adjusted by using a variable resistor. Use the data in the table to answer the questions that follow.

| **INPUT 1 (V)** | **INPUT 2 (V)** | **INPUT 3 (V)** | **$R_{IN}$ (kΩ)** | **$R_F$ (kΩ)** | **$V_{OUT}$ (V)** | **GAIN** |
|---|---|---|---|---|---|---|
| 3 | 1 | 2 | 10 | **X** | -6 | -1 |
| 0,3 | 0,4 | 0,3 | 10 | 100 | -10 | **Y** |
| 1 | 0,5 | 0,5 | 10 | 20 | **Z** | -2 |

**TABLE 3.5**

3.5.1 Determine the value of the feedback resistance ($R_F$) at **X**. (1)

3.5.2 Calculate the gain at **Y**. (3)

3.5.3 Calculate the output voltage ($V_{OUT}$) at **Z**. (3)

3.5.4 Deduce from TABLE 3.5 the relationship between $R_F$ and the gain. (1)

3.6 Refer FIGURE 3.6 below and answer the questions that follow.

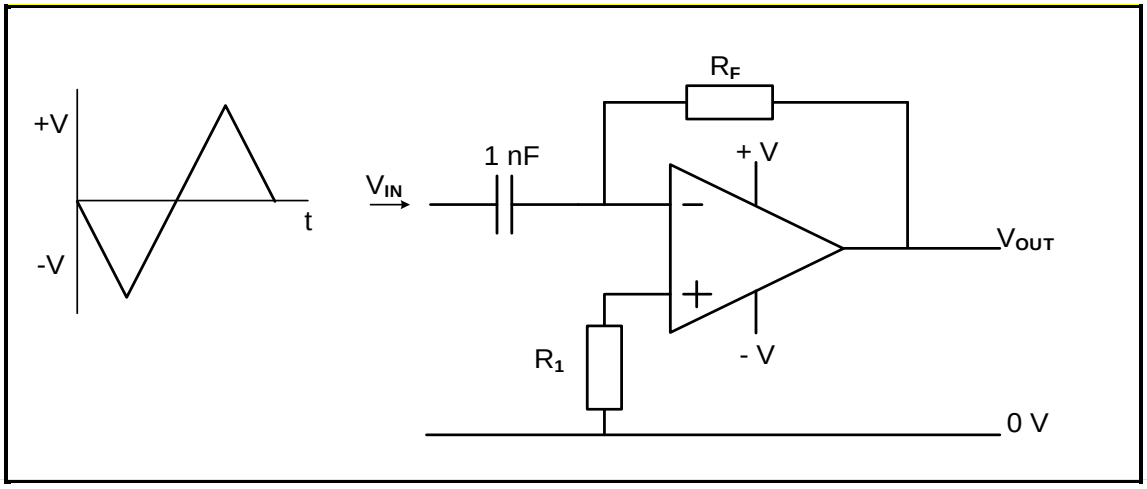



**FIGURE 3.6: OP-AMP DIFFERENTIATOR**

3.6.1 Draw the output on the ANSWER SHEET for QUESTION 3.6.1. (4)

3.6.2 Explain what determines the polarity of the output voltage. (2)
**[50]**

## QUESTION 4: SEMICONDUCTOR DEVICES

4.1 FIGURE 4.1 below shows two identical signals on the input terminals of an op amp. Draw the output waveform of the op amp in the ANSWER BOOK.

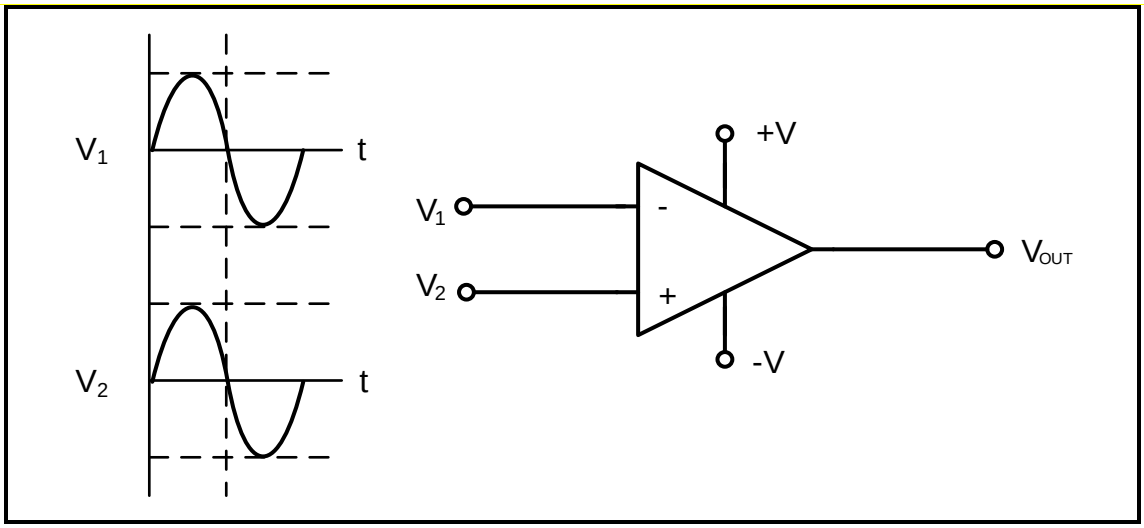



**FIGURE 4.1: 741 OP AMP** (2)

4.2 Refer to FIGURE 4.2 below and answer the questions that follow.

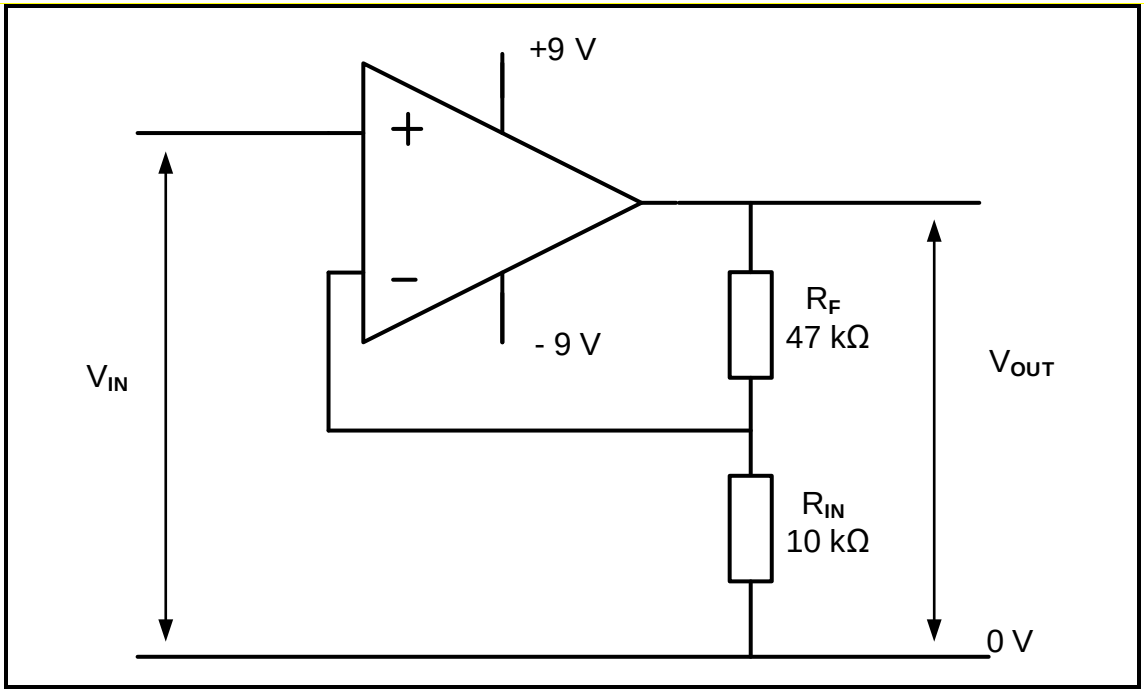



**FIGURE 4.2: OP-AMP CIRCUIT**

4.2.1 Identify the op-amp circuit in FIGURE 4.2. (1)

4.2.2 Describe what is meant by *infinite bandwidth* of an op amp. (2)

4.2.3 Calculate the voltage gain. (3)

4.2.4 Calculate the output voltage if a 100 mV signal is applied to the input. (3)

4.3 Refer to FIGURE 4.3 and answer the questions that follow.

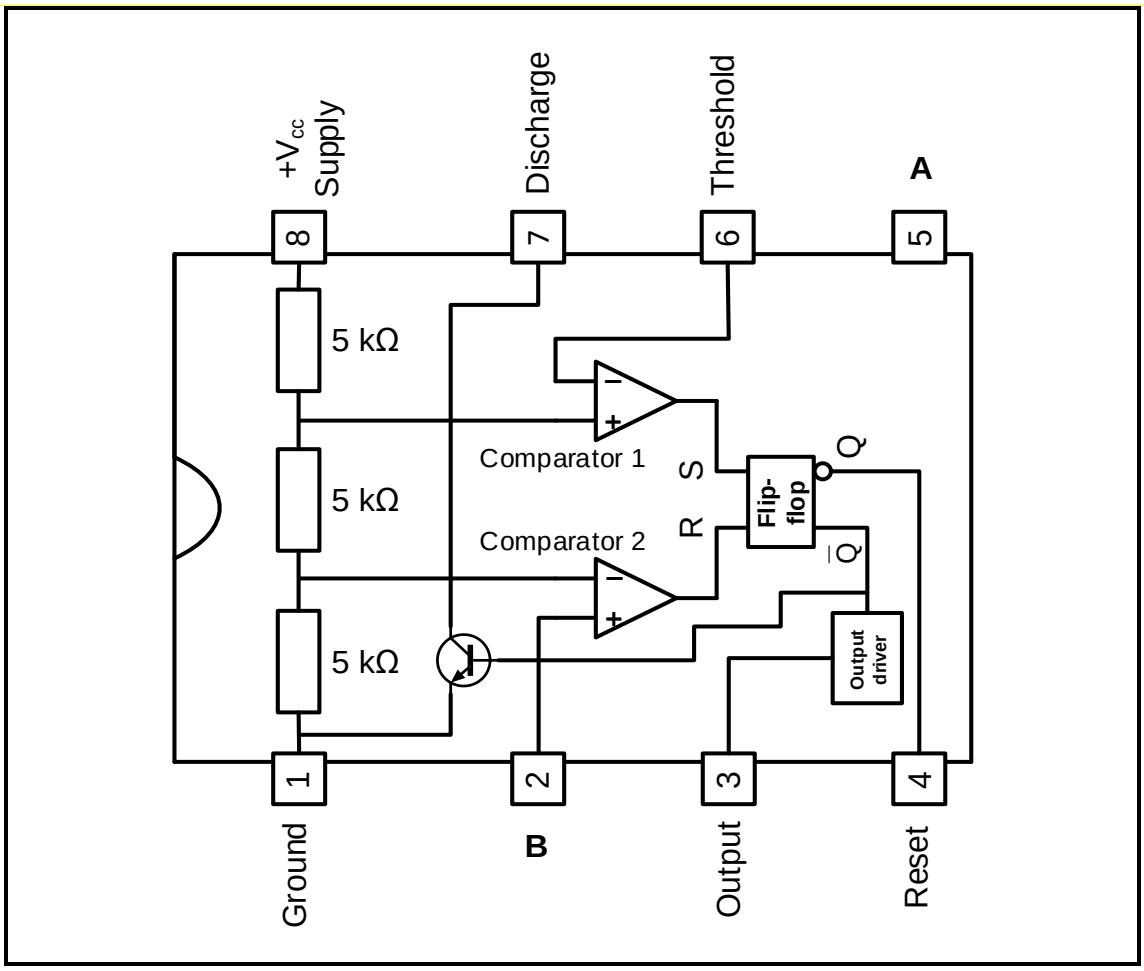



**FIGURE 4.3: 555 IC TIMER**

4.3.1 Label pins **A** and **B**. (2)

4.3.2 Explain the function of the discharge input on pin 7. (2)

4.3.3 Explain the function of comparator 1. (3)

4.3.4 State TWO uses of the 555 IC. (2)
**[20]**

## QUESTION 5: DIGITAL AND SEQUENTIAL DEVICES

5.1 Refer to an LED seven-segment display and answer the questions that follow.

5.1.1 Explain the difference between a *sinking output* and a *sourcing output*. (Drawings are NOT allowed.) (4)

5.1.2 Name ONE method, other than the LED display, of displaying information in digital systems. (1)

5.2 Refer to FIGURE 5.2 of the block diagram of a full adder below and answer the questions that follow.

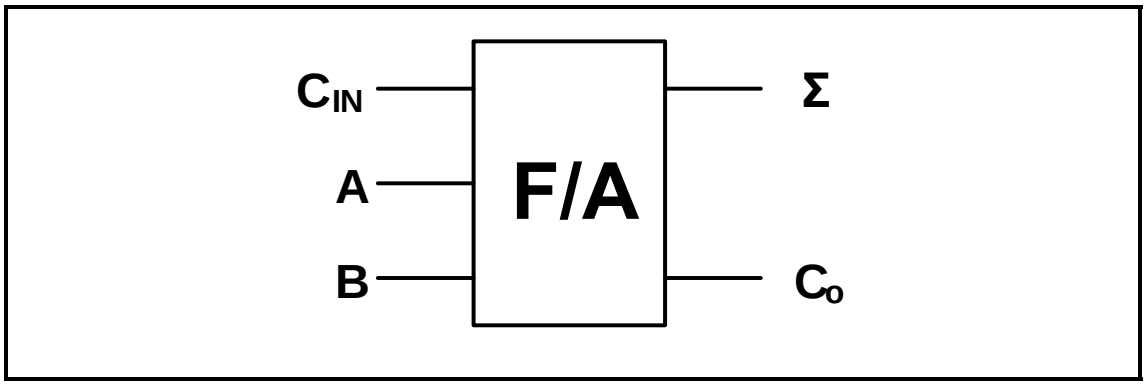



**FIGURE 5.2**

5.2.1 Complete the truth table of the full adder in TABLE 5.2.1 below on the ANSWER SHEET for QUESTION 5.2.1.

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| $C_i$ | A | B | Σ | $C_o$ |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | |
| 1 | 1 | 0 | 0 | |
| 1 | 1 | 1 | | |

**TABLE 5.2.1** (5)

5.2.2 Complete the logic circuit of the full adder on the ANSWER SHEET for QUESTION 5.2.2. (6)

5.3 Define an *asynchronous device* with reference to elementary principles of memory elements. (2)

5.4 Refer to FIGURE 5.4 of a clocked D-type flip-flop below and answer the questions that follow.

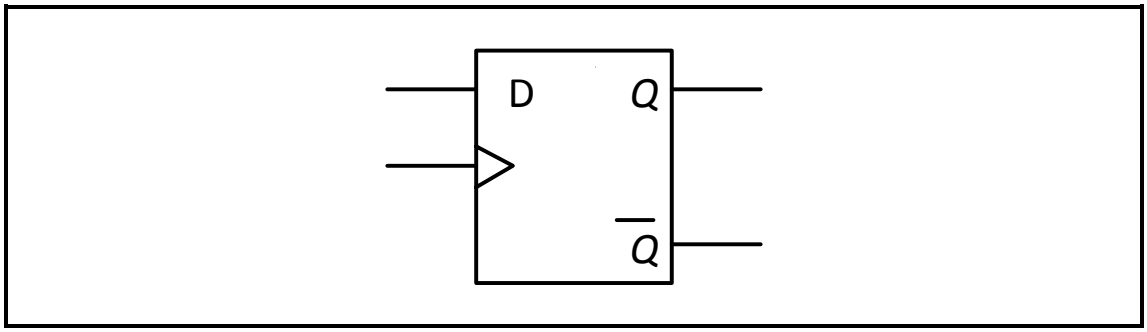



**FIGURE 5.4: D-TYPE FLIP-FLOP**

5.4.1 Complete the logic circuit of this flip-flop on the ANSWER SHEET for QUESTION 5.4.1. (6)

5.4.2 State TWO applications of D-type flip-flops in digital systems. (2)

5.4.3 Complete the timing diagrams of the flip-flop in FIGURE 5.4 on the ANSWER SHEET for QUESTION 5.4.3. Assume that Q starts low. (4)

5.5 Explain how data is moved through the series-in: series-out register. (2)

5.6 Refer to FIGURE 5.6 of a binary counter below and answer the questions that follow.

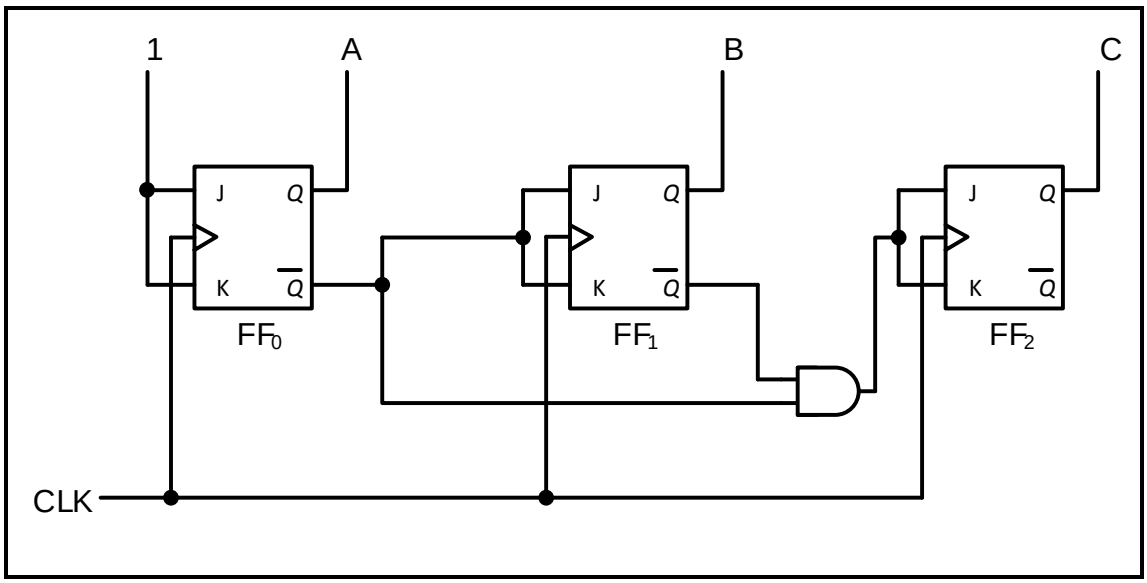



**FIGURE 5.6: BINARY COUNTER**

5.6.1 Identify the type of counter in FIGURE 5.6. (1)

5.6.2 Complete the timing diagrams for the counter in FIGURE 5.6 below on the ANSWER SHEET for QUESTION 5.6.2.

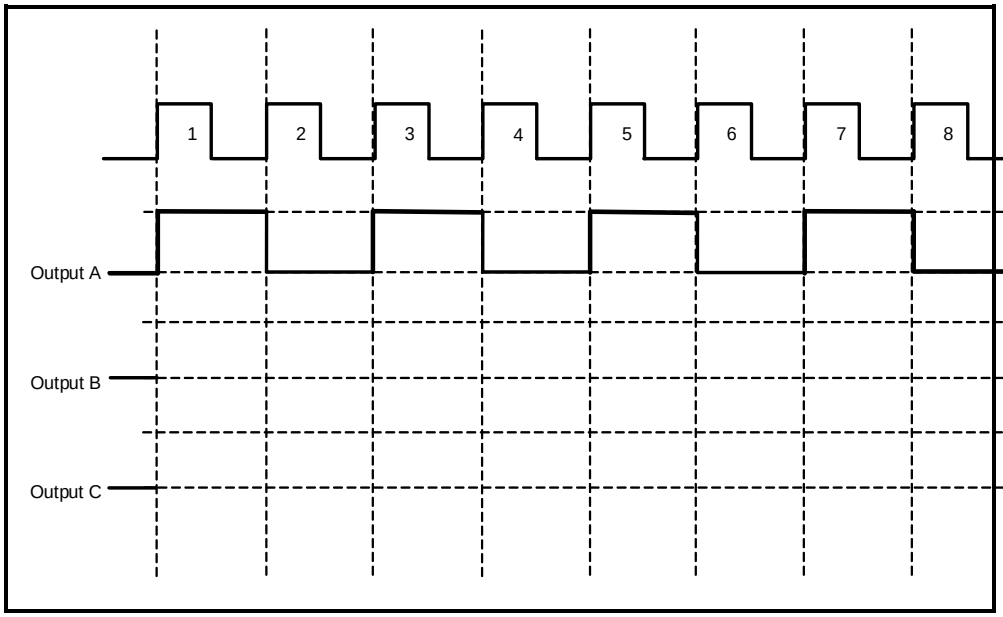



**FIGURE 5.6.2: TIMING DIAGRAMS** (8)

5.7 Refer to FIGURE 5.7 below and complete the output frequency waveforms in FIGURE 5.7 on the ANSWER SHEET for QUESTION 5.7.

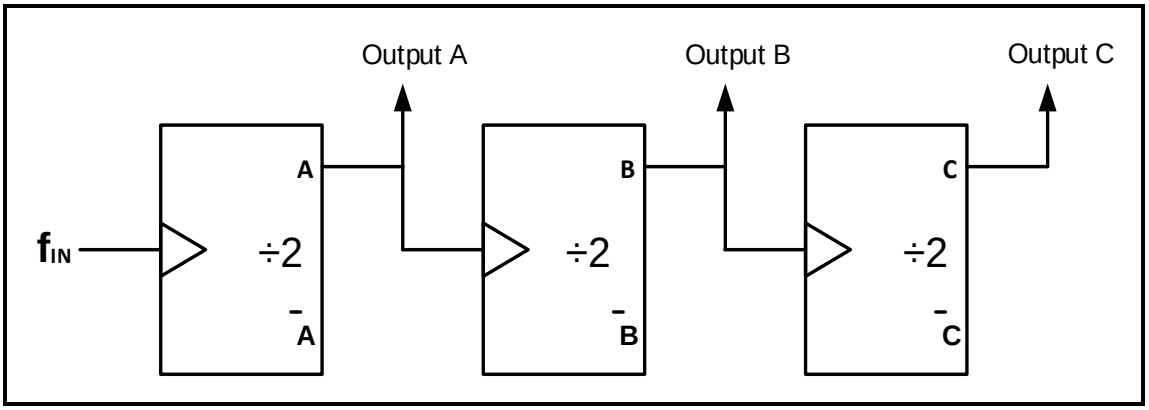



**FIGURE 5.7: FREQUENCY DIVIDER** (6)

5.8 Draw a neatly labelled sketch of a 4-bit series-in: parallel-out shift register using D-type flip-flops. Show ALL the inputs and outputs. (8)

**[55]**

## QUESTION 6: MICROCONTROLLERS

6.1 Explain how microprocessors provide digital processing control to appliances. (5)

6.2 FIGURE 6.2 below shows a CPU with registers as part of microcontrollers. Answer the questions that follow.

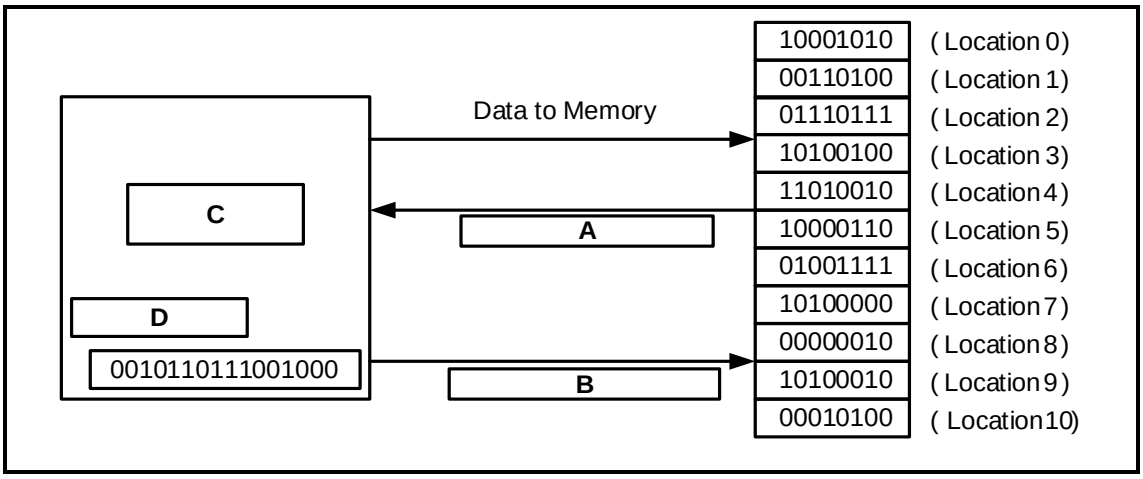



**FIGURE 6.2**

6.2.1 Label **A** to **D** in FIGURE 6.2. (4)

6.2.2 Explain the operating cycle of the CPU. (4)

6.3 Refer to registers within a CPU and explain the function of the following:

6.3.1 Memory address register (MAR) (1)

6.3.2 Program counter (PC) (3)

6.4 State the function of the cache memory. (2)

6.5 Refer to FIGURE 6.5 of serial communication below and answer the questions on the next page.

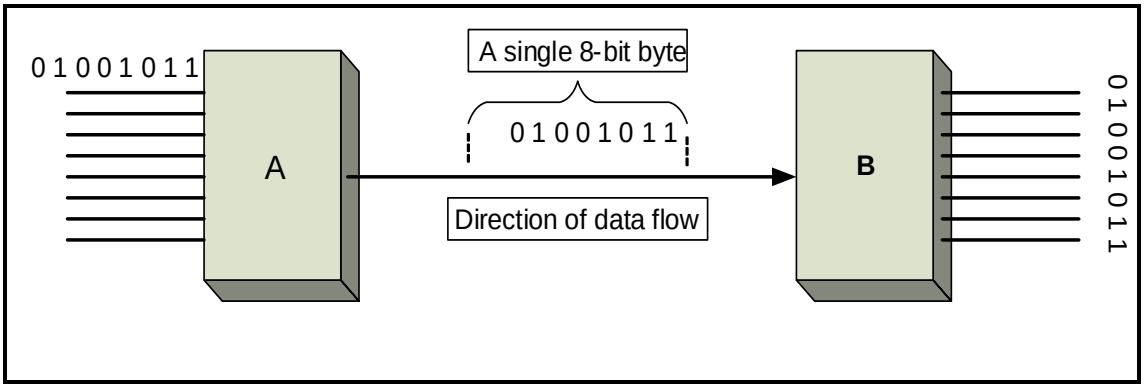



**FIGURE 6.5**

6.5.1 Label **A** and **B**. (2)

6.5.2 Explain the operation of FIGURE 6.5. (6)

6.6 State TWO advantages of the serial communication interface (SCI). (2)

6.7 Refer to FIGURE 6.7 of the inter-integrated bus (I2C) below and answer the questions that follow.

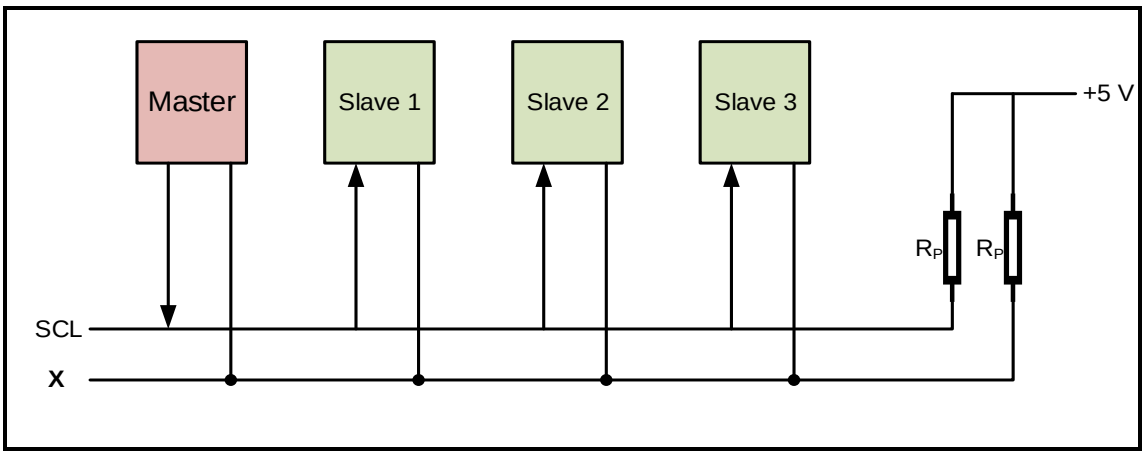



**FIGURE 6.7: INTER-INTEGRATED BUS**

6.7.1 Label line **X**. (1)

6.7.2 State TWO disadvantages of the inter-integrated bus (I2C). (2)

6.7.3 State the function of pull-up resistors $R_P$. (1)

6.7.4 Differentiate between the function of the *master* and the *slave* in FIGURE 6.7. (3)

6.8 Refer to the software of microcontrollers and explain the difference between an *algorithm* and a *program*. (4)

6.9 Study the following algorithm and complete its flow chart in FIGURE 6.9 on the ANSWER SHEET for QUESTION 6.9:

- A monostable device has one stable state.
- It changes state when it is triggered by an input.
- It stays in that state for five seconds.
- The output returns to its original state.
- The device has a single output. (10)

**[50]**

**TOTAL: 200**

## FORMULA SHEET

### SEMICONDUCTOR DEVICES

Gain $A_V = \frac{V_{OUT}}{V_{IN}} = -\left(\frac{R_F}{R_{IN}}\right)$ **OR** $A_V = 1 + \frac{R_F}{R_{IN}}$

$V_{OUT} = V_{IN} \times \left(-\frac{R_F}{R_{IN}}\right)$

$V_{OUT} = V_{IN} \times \left(1 + \frac{R_F}{R_{IN}}\right)$

### SWITCHING CIRCUITS

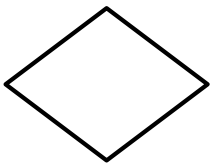
$V_{OUT} = -\left(V_1 \frac{R_F}{R_1} + V_2 \frac{R_F}{R_2} + ...V_N \frac{R_F}{R_N}\right)$

Gain $A_V = \frac{V_{OUT}}{V_{IN}} = \frac{V_{OUT}}{(V_1 + V_2 + ...V_N)}$

$V_{OUT} = -(V_1 + V_2 + ...V_N)$

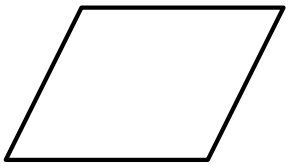
### FLOW CHART SYMBOLS USED IN PICAXE

Process

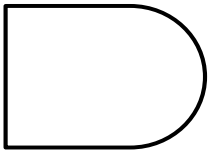


Decision

Terminator



Data



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**ANSWER SHEET**

## QUESTION 3: SWITCHING CIRCUITS

3.3.6

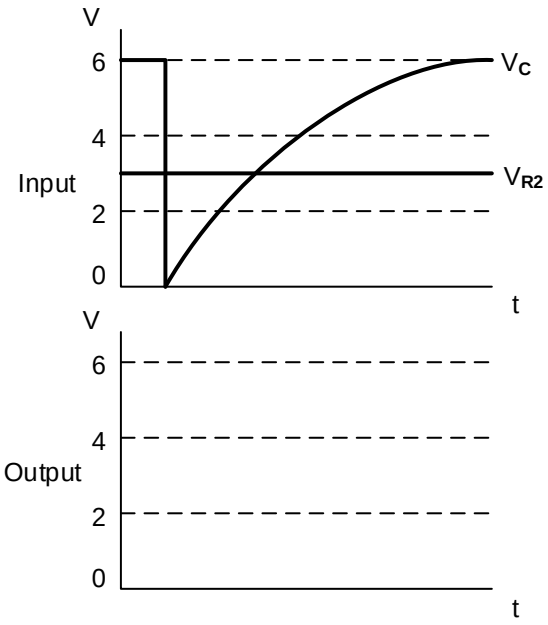


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**FIGURE 3.3.6** MOD (3)

3.4.3

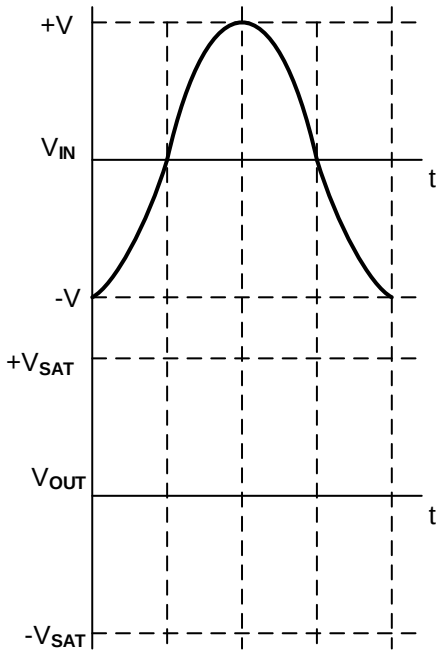


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**FIGURE 3.4.3** MOD (4)

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**ANSWER SHEET**

3.6.1

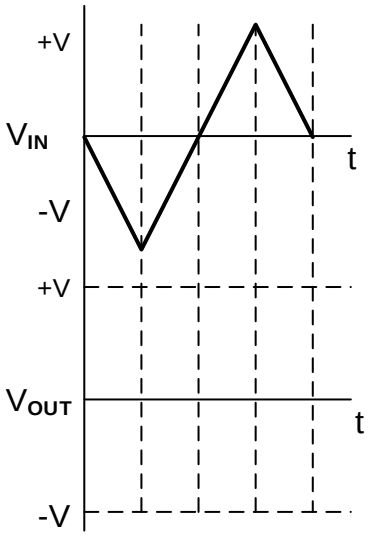


**FIGURE 3.6.1**

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MOD (4)

| **CENTRE NUMBER:** | | | | | | | |
|---|---|---|---|---|---|---|---|

| **EXAMINATION NUMBER:** | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**ANSWER SHEET**

## QUESTION 5: DIGITAL AND SEQUENTIAL DEVICES

5.2.1

| **INPUTS** | | | **OUTPUTS** | |
|---|---|---|---|---|
| **$C_i$** | **A** | **B** | **Σ** | **$C_o$** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | |
| 1 | 1 | 0 | 0 | |
| 1 | 1 | 1 | | |

**TABLE 5.2.1**

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MOD (5)

| **CENTRE NUMBER:** | | | | | | | |
|---|---|---|---|---|---|---|---|

| **EXAMINATION NUMBER:** | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**ANSWER SHEET**

5.2.2

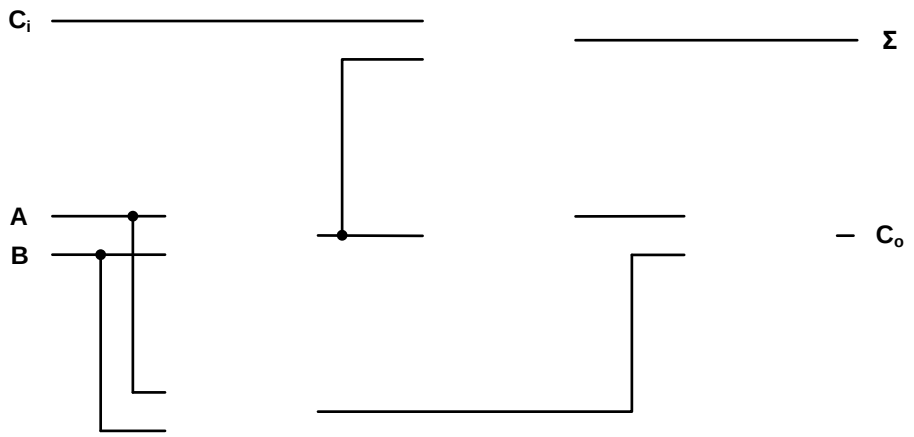


**FIGURE 5.2.2**

Transfer mark to answer book

MOD (6)

5.4.1

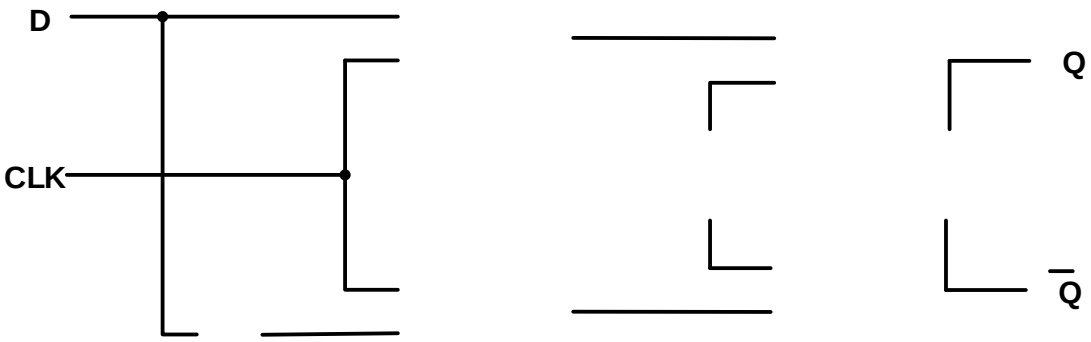


**FIGURE 5.4.1**

Transfer mark to answer book

MOD (6)

| **CENTRE NUMBER:** | | | | | | | |
|---|---|---|---|---|---|---|---|

| **EXAMINATION NUMBER:** | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**ANSWER SHEET**

5.4.3

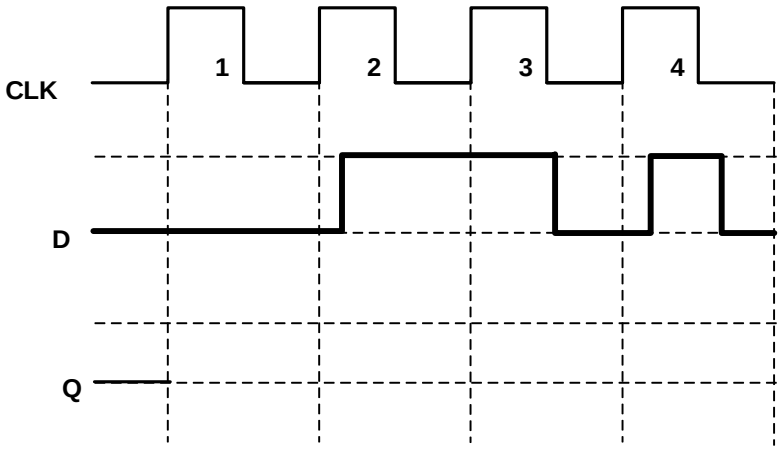


**FIGURE 5.4.3**

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MOD (4)

| **CENTRE NUMBER:** | | | | | | | |
|---|---|---|---|---|---|---|---|

| **EXAMINATION NUMBER:** | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**ANSWER SHEET**

5.6.2

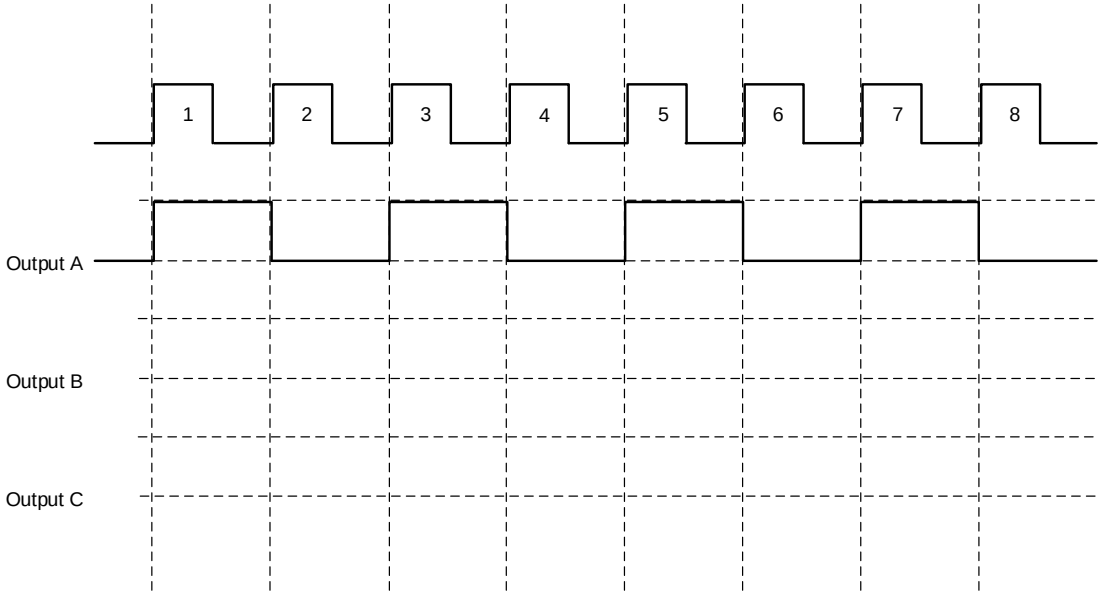


**FIGURE 5.6.2**

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MOD

(8)

| **CENTRE NUMBER:** | | | | | | | |
|---|---|---|---|---|---|---|---|

| **EXAMINATION NUMBER:** | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

**ANSWER SHEET**

5.7

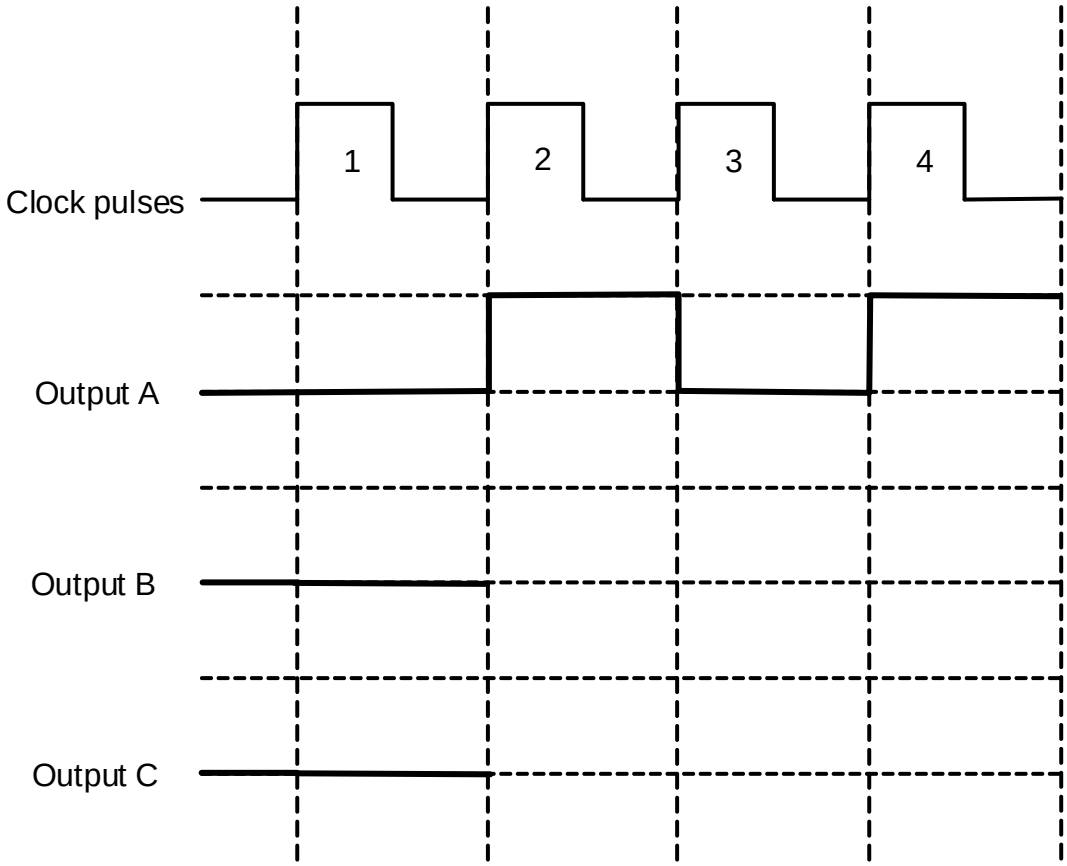


**FIGURE 5.7**

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MOD

(6)

| **CENTRE NUMBER:** | | | | | | | |
|---|---|---|---|---|---|---|---|

| **EXAMINATION NUMBER:** | | | | | | | | | | | | | |
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**ANSWER SHEET**

**QUESTION 6: MICROCONTROLLERS**

6.9

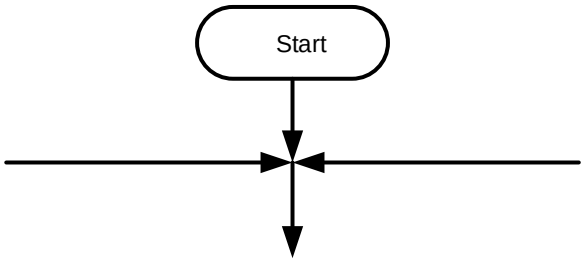


**FIGURE 6.9**

Transfer mark to answer book

MOD (10)